United States Patent and Trademark Office

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09/829,146	04/09/2001	Thomas N. Toombs	M-10234-1D US	1045

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EXAMINER
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ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>27 March 2006</u>.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *18-19, 22, 24 –31, and 33-41* is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) *33* is/are allowed.

6) ☒ Claim(s) *18-19, 22, 24 –31, and 34-41* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a) ☐ All   b) ☐ Some * c) ☐ None of:

        1. ☐ Certified copies of the priority documents have been received.

        2. ☐ Certified copies of the priority documents have been received in Application No. _____.

        3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
     Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

Detailed Action

1.   Claims 18-19, 22, 24 –31, and 33-41 are presented for examination.   This office

action is in response to the amendment filed on 3/27/06.

2.   Applicant is requested to particularly point out the figure number(s) in the drawing

and (corresponding) line number(s) and page number(s) in the specification that is

specifically directed to each claimed invention, e.g. the number of memory cells in each

memory group is configurable, wherein the corresponding cells in each memory group

are calculated in real time.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 37-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Flash

Memory Products, 1992/1993 Data Book/Handbook, Advanced Micro Devices,

Am29F010, pp1-3 thru 1-16, 1-25, 1-26, 1-27, 3-38 thru 3-60, and 3-71 (AMD).

As to claim 37, AMD discloses the invention as claimed. AMD discloses a

memory system (1-4) comprises a plurality of memory groups (sectors 1-4), each of

said memory groups comprising a plurality of memory cells (cell matrix in 1-4); a

plurality of group tags (table 4), each of said group tags corresponding to one of said

memory groups, each of said group tags indicating whether the memory cells under the

corresponding memory group are write protected (1-3 "disables any combination of

sectors from program" reads on this limitation since it would avoid writing

(programming) to designated sectors); and wherein any combination of the memory

groups can be write protected (1-3 disables any combination of sectors from program

reads on this limitation) and said group tags are settable in response to a command

from a host to which the memory system is connected (Table 4 and 1-10 Sector

Protection " The sector protect feature is enabled using programming equipment" reads

on this limitation since it would require programming input from a processor).

As to claim 38, AMD further discloses set ones said group tags are deselected in

response to command from said host (table 4, 1-3 disables any combination of sectors

from program reads on this limitation and 1-10, Sector Protection section).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 24, 26, 34-36, 25, and 27 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Flash Memory Products, 1992/1993 Data Book/Handbook, Advanced

Micro Devices, Am29F010, pp1-3 thru 1-16, 1-25, 1-26, 1-27, 3-38 thru 3-60, and 3-71

(AMD) in view of Hazen et al. (Hazen) U.S. Patent No. 5,280,447 or Lee et al. (Lee)

U.S. Patent No. 5,796,657.

As to claim 24, AMD discloses the invention as claimed. AMD discloses a

memory system (1-4) comprises a plurality of memory groups (sectors in 1-4), each of

said memory groups comprising a plurality of memory cells (cell matrix in 1-4); a

plurality of group tags (table 4), each of said group tags corresponding to one of said

memory groups, each of said group tags indicating whether the memory cells under the

corresponding memory group are write protected (1-3 "disables any combination of

sectors from program" reads on this limitation since it would avoid writing

(programming) to designated sectors); and wherein any combination of the memory

groups can be write protected (1-3 "disables any combination of sectors from program"

reads on this limitation).

However, AMD does not specifically disclose the number of memory cells in each

memory group is configurable.

Hazen discloses the number of memory cells in each memory group is

configurable (col. 4 lines 39-42) for the purpose of providing capability of the size of

each blocks of the flash can be selected by a user of the flash (col. 4 lines 40-42).

Therefore, it would have been obvious to one having ordinary skill in the memory

art at the time the invention was made to incorporate the number of memory cells in

each memory group is configurable as shown in Hazen into the invention of AMD for the

advantages stated above.

Alternatively, Lee discloses the number of memory cells in each memory group is configurable (col. 3 lines 30-40 and col. 5 lines 13-16) for the purpose of providing capability flexible erasing size and enhancing the performance.

Therefore, it would have been obvious to one having ordinary skill in the memory art at the time the invention was made to incorporate the number of memory cells in each memory group is configurable as shown in Lee into the invention of AMD for the advantages stated above.

As to claim 25, AMD discloses the invention as claimed. AMD discloses a memory system (1-4) comprises a plurality of memory groups (sectors in 1-4), each of said memory groups comprising a plurality of memory cells (cell matrix in 1-4); a plurality of group tags (Table 4), each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are write protected (1-3 disables any combination of sectors from program reads on this limitation since it would avoid writing(programming) to designated sectors); and wherein any combination of the memory groups can be write protected (1-3 disables any combination of sectors from program reads on this limitation).

However, AMD does not specifically disclose the corresponding cells in each memory groups is calculated in real time.

Hazen discloses the corresponding cells in each memory groups is calculated in real time (col. 4 lines 25-42, since configuration cell should be programmed by applying

control signals externally) for the purpose of the purpose of providing capability of the

size of each blocks of the flash can be selected by a user of the flash (col. 4 lines 40-

42). Therefore, it would have been obvious to one having ordinary skill in the memory

art at the time the invention was made to incorporate the corresponding cells in each

memory groups is calculated in real time as shown in Hazen into the invention of AMD

for the advantages stated above.

Alternatively, Lee discloses the corresponding cells in each memory groups is

calculated in real time (col. 5 lines 30-50. col. 3 lines 30-40 and col. 5 lines 13-16, since

control signals should be provided externally) for the purpose of providing capability

flexible erasing size and enhancing the performance.

Therefore, it would have been obvious to one having ordinary skill in the memory

art at the time the invention was made to incorporate the corresponding cells in each

memory groups is calculated in real time as shown in Lee into the invention of AMD for

the advantages stated above.

As to claims 26 and 27, AMD further discloses a flash memory (1-3).

As to claim 34, AMD further discloses wherein said group tags are settable by a

host to which the memory system is connected (Table 4 and 1-10 Sector Protection "

The sector protect feature is enabled using programming equipment" reads on this

limitation since it would require programming input from a processor).

As to claim 35, AMD further discloses wherein said group tags are set in

response to a host command (Table 4 and 1-10 Sector Protection " The sector protect

feature is enabled using programming equipment" reads on this limitation since it would

require programming input from a processor).

As to claim 36, AMD further discloses wherein set ones of said group tags are

deselected in response to a host command (Table 4 and 1-3 disables any combination

of sectors from program reads on this limitation and 1-10, Sector Protection section).

5.   Claims 18–19, 22, 28-31, and 39-41 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Flash Memory Products, 1992/1993 Data Book/Handbook,

Advanced Micro Devices, Am29F010, pp1-3 thru 1-16, 1-25, 1-26, 1-27, 3-38 thru 3-60,

and 3-71 (AMD) in view of Kaki et al. (Kaki) U. S. Patent 5,809,515.

As to claim 18, AMD discloses a memory system (3-39) comprises a plurality of

memory groups (S0-S7 in 3-39), each of the memory groups comprising a plurality of

memory sectors (1-4), each of the memory sectors comprising a plurality of memory

cells (cell matrix in 1-4) wherein the number of memory sectors in each memory group

is configurable (1-3, "disables any combination of sectors from programming or erase

operation" reads on this limitation); a plurality of sector tags (any combination of sectors

can concurrently erased in 1-3 reads on this limitation since it need to be programmed

and "command (data) is latched" as descried in Sector Erase section in 1-12), each of

the sector tags corresponds to a memory sector, each of the sector tags indicating

whether the memory cells under the corresponding memory sector are erasable, wherein al the memory cells belong to one memory sector are erasable when the corresponding sector tag is set, wherein any combination of memory sectors in a memory group can be simultaneously erased (1-3). Although AMD discloses full chip erase (1-3), however, AMD does not specifically disclose a plurality of group tags, each of the group tags corresponds to one of the memory groups, each of the group tags indicating whether the memory cells under the corresponding memory group are erasable, wherein al the memory cells belong to one memory group are erasable when the corresponding group is set, wherein any combination of memory groups can be simultaneously erased.

Kaki discloses a plurality of group tags, each of the group tags corresponds to one of the memory groups, each of the group tags indicating whether the memory cells under the corresponding memory group are erasable (col. 7 line 64 thru col. 8 line 14), wherein all the memory cells belong to one memory group are erasable when the corresponding group is set, wherein any combination of memory groups can be simultaneously erased (col. 7 lines 28-30, "Thus, the plurality of flash memories 4 are erased in parallel" reads on this limitation) for the purpose of increasing the memory erasing speed thereby increasing the access bandwidth.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate plurality of group tags, each of the group tags corresponds to one of the memory groups, each of the group tags indicating whether the memory cells under the corresponding memory group are erasable,

wherein all the memory cells belong to one memory group are erasable when the

corresponding group is set, wherein any combination of memory groups can be

simultaneously erased as shown in Kaki into the invention of AMD because it would

increase the memory access speed.

As to claim 19, AMD and Kaki disclose the invention as claimed above. AMD

further discloses the corresponding sectors in each memory group is calculated in real

time (1-25, sector protection algorithms reads on this limitation, since it requires external

signal sequences from a processor).

As to claim 22, AMD and Kaki disclose the invention as claimed above. AMD

further discloses a flash memory (1-3)

As to claim 28, AMD and Kaki disclose the invention as claimed above. The

sector tags (disclosed by AMD, any combination of sectors can concurrently erased in

1-3 reads on this limitation since it need to be programmed and "command (data) is

latched" as descried in Sector Erase section in 1-12) and the group tags (disclosed by

Kaki Fig. 4 Refs. 42-47) are settable by a host to which the memory system is

connected.

As to claim 29, AMD and Kaki disclose the invention as claimed above. AMD

further discloses the sector tags are set in response to a host command (1-12 "Sector

erase is a six bus cycle in sector erase" reads on this limitation).

As to claim 30, AMD and Kaki disclose the invention as claimed above. AMD

further discloses the sector tags and the group tags are deselected in response to a

host command (1-25, Sector protection algorithms).

As to claim 31, AMD and Kaki disclose the invention as claimed above. AMD

further discloses wherein the number of memory sectors in each memory group is

configurable (1-25, disables any combination of sectors) by a host to which the memory

system is connected (1-25, sector protection algorithms reads on this limitation, since it

requires external signal sequences from a processor).

As to claim 39, AMD discloses a method of operating a memory card (3-39) that

includes a memory array (S0-S7 in 3-39) formed of a plurality of unit of erase (1-4,

sector), each which is composed of a plurality of memory cells (cell matrix in 1-4), the

method comprises organizing the memory into a plurality of memory groups (S0-S7 in

3-39), each of said memory groups comprising a plurality of units of erase, (1-4 sector)

wherein all the memory cells belonging to one of said units of erase memory sector are

erasable when either the corresponding unit of erase or the corresponding group of the

units of erase is selected (1-3 "any combination of sectors can be concurrently erased

Also supports full chip erase), and wherein any combination of units of erase in a

memory group can be simultaneously erased 1-3 "any combination of sectors can be

concurrently erased Also supports full chip erase).

Although AMD discloses full chip erase (1-3), however, AMD does not

specifically disclose any combination of the memory groups can be simultaneously

erased.

Kaki discloses any combination of the memory groups can be simultaneously

erased (col. 7 line 64 thru col. 8 line 14 and col. 7 lines 28-30, "chip unit" and "Thus, the

plurality of flash memories 4 are erased in parallel" read on this limitation) for the

purpose of increasing the memory erasing speed thereby increasing the access

bandwidth.

Therefore, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to incorporate any combination of the memory groups

can be simultaneously erased as shown in Kaki into the invention of AMD because it

would increase the memory access speed.

As to claim 40, AMD and Kaki disclose the invention as claimed above. AMD

further discloses wherein the size of the groups is configurable by a host to which the

card is connected. (3-49, program set-up/program command)

As to claim 41, AMD and Kaki disclose the invention as claimed above. AMD

further discloses wherein the size of the groups is stored in a register on card.

Allowable Subject Matter

6.   Claim 33 is allowed.

Response to Arguments

7.   Applicant's arguments filed on 3/27/06 have been fully considered but they are

not deemed to be persuasive.

Applicant's remarks that the references not teaching write protection and group

tags are not considered persuasive.

AMD discloses write protection (page 1-10, sector protection) and group tags

(table 4).

Hazen also discloses "One of the objects of the present invention is to provide a

nonvolatile memory that is organized into blocks, wherein the size and the number of

the blocks can be altered. Another object of the present invention is to provide a

nonvolatile memory with blocks with improved erasure characteristics. Another object

of the present invention is to provide a nonvolatile memory that is organized into

blocks, wherein the size and the number of the blocks are user configurable. Another

object of the present invention is to provide a nonvolatile memory that is organized into

blocks, wherein current hogging of memory cells in a block during erasing is minimized

(col. 2 lines 56+).

Therefore broadly written claims are disclosed by the references cited.

Conclusion

1.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.   See attached PTO-892.

2.   A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3.   When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections.   See 37 C.F.R. ' 1.111(c).

4.   When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

    If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should

be directed to the TC 2100 whose telephone number is (571) 272-2100.

6.   Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

7.   **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
571-273-8300

Hand-delivered responses should be brought to the Customer Service
Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK
Primary Patent Examiner
April 11, 2006